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10/518,991	12/21/2004	Richard Michael Taylor	5035-199US//P29650-USA	7639

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SYNNESTVEDT LECHNER & WOODBRIDGE LLP
P O BOX 592
112 NASSAU STREET
PRINCETON, NJ 08542-0592

EXAMINER	
WHITMORE, STACY	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/518,991	TAYLOR, RICHARD MICHAEL	
	Examiner	Art Unit	
	Stacy A. Whitmore	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-23 and 26-34* is/are rejected.

7)☒ Claim(s) *7,24 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/11/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 8-13, 18, 22-23, 26, and 28-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

I. As for claims 22, 26, and 30, applicant claims "may be", which is unclear because the claim limitations may or may not be part of the claimed limitations.

II. Claim 8 recites the limitation "candidate" in line 1. There is insufficient antecedent basis for this limitation in the claim.

III. Claim 18 recites the limitation "the fitness metric" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

IV. Claim 28 recites the limitation "the stored information" and " the execution word layout" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

V. Claim 29 recites the limitation "the selection codes" in line 2. There is insufficient antecedent basis for this limitation in the claim.

VI. Claim 30 recites the limitation "the information stored" in line 2. There is insufficient antecedent basis for this limitation in the claim.

VII. Claim 31 recites the limitation "the required package or library files" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

VIII. Claim 32 recites the limitation "the weighting" in line 2. There is insufficient antecedent basis for this limitation in the claim.

IX. Claim 33 recites the limitation "the weighting" and "the profile weighting" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-6, 8-10, 14-17, 19-23, 26-30, and 34 are rejected under 35 U.S.C. 102(e) as being anticipated by Master (US Patent Application Publication 2006/0031660).

3. As for the claims, Master discloses the invention as claimed, including:

1. (Currently amended) A method of automatic configuration of a microprocessor architecture whereby:

(a) the architecture includes a configurable number of execution units [abstract];

(b) the architecture has configurable connectivity between those execution units [abstract, fig. 5];

(c) the execution units are able to communicate data directly without the need to be connected between register files that are shared between multiple execution units

[abstract, fig. 5, paragraphs 0010, 0013, 0030-0034, 0048, 0052]; and
(d) the data and control flows within a particular input program are used to influence decisions regarding execution unit replication and connectivity [Fig. 1; abstract, fig. 5, paragraphs 0010, 0013, 0030-0034];
2. (original) The method according to claim 1 whereby multiple candidate architectures are generated [paragraphs 0009, 0027, 0052];
3. (original) The method according to claim 2 whereby the best candidate architecture is automatically selected on the basis of user defined metrics [paragraph 0010];
4. (original) The method according to claim 2 whereby data is output to allow the construction of a graph representing the characteristics of certain candidates [paragraphs 0074-0075];
5. (original) The method according to claim 2 whereby a number of new connections and or execution units are added to the architecture on each generation [paragraphs 0009-0010, 0027, 0048, 0052];
6. (original) The method according to claim 5 whereby mapping of code onto a trial architecture is used to influence connectivity choices [paragraph 0082, for example, shows that mapping of configuration data (code as shown in fig. 1, may be loaded according to changing modes of operation (or trial architectures that can change as needed)];
8. (original) The method according to claim 1 whereby every candidate generated contains a certain minimum set of execution unit types [abstract; fig. 5, paragraphs 0009-0010, 0027, 0048, 0052 – a minimum set of execution unit types is generated to meet the specific application requirement];
9. (original) The method according to claim 8 whereby there is a certain minimum connectivity between all execution units [abstract; fig. 5, paragraphs 0009-0010, 0027, 0048, 0052 – a minimum connectivity between execution unit types is generated to meet the specific application requirement];
10. (original) The method according to claim 9 whereby the minimum connectivity guarantees that arbitrary new code sequences can be mapped to the architecture [abstract; fig. 5, paragraphs 0009-0010, 0027, 0048, 0052 – a minimum connectivity

between execution unit types is generated to meet the specific application requirement, and any code can be mapped to the units based on configuration];

14. (original) The method according to claim 1 whereby the initial connectivity within the architecture is determined from data flows within graph representations of the input program [paragraphs 0074-0075, the DFGs as shown which are utilized to configure the chip originates from the program code of fig. 1 that is used to configure the chip];

15. (original) The method according to claim 5 whereby the new connections are added as a result of connections requested during the code generation process [fig. 1; paragraphs 0009-0010, 0027, 0033-0034, 0048, 0052];

16. (original) The method according to claim 15 whereby the addition of new connections is constrained by certain rules [fig. 1; paragraphs 0009-0010, 0027, 0033-0034, 0048, 0052, the rules are provided by the user data];

17. (original) The method according to claim 16 whereby the connectivity rules relate to maximum number of operand inputs, maximum number of result outputs and the estimated connectivity distance [fig. 1; paragraphs 0009-0010, 0027, 0033-0034, 0048, 0052, 0100-0101, the rules, operand, and result output configurations are provided by the user data and have an inherent maximum based on the configuration and spatial and temporal information];

19. (original) The method according to claim 1 whereby the execution units are placed in a logical grid layout [fig. 5, paragraph 0052 – matrix layout and/or FPGA style layout];

20. (original) The method according to claim 19 whereby the connectivity rules include a maximum distance between execution unit grid positions [fig. 5, paragraph 0052 – matrix layout and/or FPGA style layout; paragraphs 0100-0101 – spatial and temporal configuration information];

21. (original) The method according to claim 19 whereby the execution units are obtained from a component library, each of which includes a reference to the hardware description of the execution unit [paragraphs 0041-0042 show that the units may be configured, or obtained from information stored on a network, "stored as hardware on the net" – thus the information being stored in a file or library];

22. (original) The method according to claim 21 whereby the execution unit components have pre-characterized characteristics [paragraphs 0041-0042 show that the units may be configured, or obtained from information stored on a network, "stored as hardware on the net" – thus the information being stored in a file or library and inherently being pre-stored, have pre-characterized characteristics] that may include area, maximum operational frequency and average power consumption [paragraph 0027 – power optimization];

Note, the claim limitation "may include" is not necessarily a claim limitation, and therefore is not required by the rejection.

23. (original) The method according to claim 22 whereby each architecture is designed to have a minimum operational frequency on a given implementation technology [paragraph 0032, clocking configuration is a minimum operating frequency for the configured technology, at least by controlling various configurations to operate at a particular clock rate];

26. (original) The method according to claim 1 whereby the architecture may be optimized for a certain set of functions that are specified to the system [paragraph 0027];

Note the claim limitation "may be optimized" is not necessarily a claim limitation, and therefore is not required by the rejection.

27. (original) The method according to claim 1 whereby the number and type of execution units and their connectivity for a given architecture is stored in a description file [paragraphs 0041-0042 show that the units may be configured, or obtained from information stored on a network, "stored as hardware on the net" – thus the information being stored in a description file or library and inherently being pre-stored, have pre-characterized characteristics];

28. (original) The method according to claim 27 whereby the stored information includes details of the execution word layout used to control each of the execution units [fig. 1; paragraphs 0041-0042 show that the units may be configured, or obtained from information stored on a network, "stored as hardware on the net" – thus the information being stored in a file or library and inherently being pre-stored, have pre-characterized

characteristics; and paragraph 0036 showing the word layout as encoded by a number of bits (or word layout)];

29. (original) The method according to claim 28 whereby the stored information includes details of the selection codes associated with operand inputs, output registers and execution unit operation codes [fig. 1, paragraphs 0033; 0076 showing output registers of units, which are also configured by the code];

30. (original) The method according to claim 27 whereby a top level hardware description language file may be generated from the information stored that instantiates connectivity and required execution units [paragraphs 0041-0042 show that the units may be configured, or obtained from information stored on a network, "stored as hardware on the net" – thus the information being stored in a description file or library and inherently being pre-stored, have pre-characterized characteristics, the stored information on the network may be viewed as a top level description];

34. (Previously presented) A microprocessor automatically configured using a method as defined in Claim 1 [abstract].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Master (US Patent Application Publication 2006/0031660) in view of Killian (US Patent Application Publication 2006/0259878).

5. As for the claims, Master discloses the invention substantially as claimed, including the method of automatic configuration of a microprocessor architecture as cited above in the rejections of claims 1 and 27. Master also discloses whereby the required package or library files are automatically generated to incorporate the hardware descriptions [paragraphs 0041-0042 show that the units may be configured, or obtained from information stored on a network, "stored as hardware on the net" – thus the information being stored in a description file or library and inherently being pre-stored, have pre-characterized characteristics];

Master does not specifically disclose hardware synthesis as in claim 31;
32. (original) The method according to claim 31 whereby instruction level profiling information is used to influence the weighting of individual instructions;
33. (original) The method according to claim 32 whereby the weighting of individual instructions during scheduling is related to the profile weighting.

Killian discloses HDL synthesis [paragraph 0007];
32. (original) The method according to claim 31 whereby instruction level profiling information is used to influence the weighting of individual instructions [paragraphs 0176 and 0178];
33. (original) The method according to claim 32 whereby the weighting of individual instructions during scheduling is related to the profile weighting [paragraphs 0176 and 0178].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Master and Killian because utilizing an HDL synthesis for Master's system would have provided Master's system with a well known

design language that is portable and used widely in industry, thereby allowing Master's system of design a wider range of potential users. Further, using instruction level profiling and weighting during scheduling in Master's system would provide Master's system a method of optimizing instruction use for improved configuration and use of configured processing units [see Killian, paragraphs 0177 and 0007-0009].

6. Claims 7, and 24-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 11-13, and 18 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to disclose either singularly or in combination the invention as claimed, including the method of automatic configuration of a microprocessor comprising at least the steps of 7. (original) The method according to claim 6 whereby the delays caused by execution unit conflicts in the schedule are used to increase the chances of an additional execution unit of that type being added to the architecture; 11. (original) The method according to claim 10 whereby the guarantee of mapping of new code is performed using a reachability analysis between results and operands within the architecture;12. (original) The method according to claim 11 whereby the reachability analysis ensures that the result of every type of execution unit can be transported to the operand of every type of execution unit; 13. (original) The method according to claim 11 whereby the reachability analysis ensures that every result can be written to a central register file and that every operand can be read from a central register file; 18. (original) The method according to claim 17 whereby a set of potential new connections are maintained and those which are added are those which will improve the fitness metric most but are within the constraints; 24. (original) The

method according to claim 19 whereby the placement of execution units is initiated with the register file at the centre of the grid; 25. (original) The method according to claim 24 whereby the placement of execution units is performed from the centre outward in order of decreasing usage frequency of the execution units.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A. Whitmore whose telephone number is (571) 272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Stacy A Whitmore/
Primary Examiner
Art Unit 2825

SAW
July 11, 2007